



PLA
UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/850,228	05/08/2001	Satoru Kishimoto	207200US2	2241
22850	7590	04/27/2004	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			PATEL, NITIN C	
		ART UNIT		PAPER NUMBER
		2116		5
DATE MAILED: 04/27/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/850,228	KISHIMOTO, SATORU
	Examiner Nitin C. Patel	Art Unit 2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-6 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. Claims 1 – 6 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 6, are rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma et al. [hereinafter as Naganuma], European Patent Publication number 0684572 A2, and further in view of Debnath et al. [hereinafter as Debnath], US Patent 5, 564, 022.

5. As to claims 1, 5, and 6, Naganuma discloses a method of placing and routing elements of semiconductor integrated circuit [IC] including synthesizing of clock tree [ST14, fig. 29] comprising the steps of temporarily placing and routing a group of elements [load cells with clock terminals] having a common input capacitance; and includes a step of replacing an element [load cells] on different reserved lines such that satisfies a target skew with respect to a driver cell [col. 1, lines 1 – 11, col. 2, lines 5 – 29, fig. 6, and 29]. However, Naganuma placing and

routing method of elements of semiconductor circuit including synthesizing of clock tree but he does not discloses in detail about verification of delay simulation with targeted value. In summary, he does not disclose a verification step for simulated value and targeted value.

Debnath teaches an invention and method related to placing and routing properly sized clock buffers to reduce clock skew by first placing clock buffers within close proximity to the local clock trunks and routing is performed to connect the clock buffers to their corresponding clock trunks and performance is evaluated. If the performance does not meet a predetermined minimum threshold then cells are modified to attain the minimum threshold by removing and replacing the clock buffers previously inserted by a new set of clock buffers, and performance is then evaluated to determine whether it meets the predetermined minimum threshold or not. If it does then process is complete otherwise above process of modifying the cells, and re-placing them, and re-inserting a new set of clock buffers is repeated until the minimum threshold is satisfied [col. 2, lines 19 – 48, col. 5 – 6, fig. 3, and 4].

It would have been an obvious to one of an ordinary skill in art at the time of invention to combine the teachings of Naganuma and Debnath as both are related to placing and routing method of semiconductor IC with reducing the clock skew and Debnath's method will change routing minimally as placement of existing cells is not modified and solve the minimum delay problems and finished a new schematic [col. 8, lines 41 – 59, col. 9, lines 58 – 64].

6. As to claims 2 – 4, Debnath teaches a selective replacement of driver element [buffer] with different driving capabilities, and a common input capacitance [col. 6, Table 1] until evaluated value of clock skew becomes equal to or smaller than target value [col. 2, lines 41 – 49, col. 5, lines 28 – 67, col. 6, 1 – 65, fig. 3, 4].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
April 22, 2004


LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 8002100